IN THE CLAIMS:

Please cancel claims 78 and 79. **Please also amend** claims 56, 59, 60, 63, 65, 67, 71, 72, and 80 as shown in the complete list of claims that is presented below:

Claims 1-55 (cancelled).

56. (currently amended) A semiconductor device comprising:

a semiconductor chip having a first chip surface and a second chip surface on which a plurality of electrode pads are formed;

a molding resin structure covering the semiconductor chip, the molding resin structure having a first main surface and a second main surface opposite to the first main surface;

a plurality of terminals formed on the first main surface of the structure, the terminals being electrically connected to the electrode pads, respectively; and

a stripe groove formed on the ~~second main surface of the structure~~ first chip surface, wherein the stripe groove divides the ~~second main~~ first chip surface asymmetrically.

57. (previously presented) A semiconductor device according to claim 56, wherein the stripe groove has a V shaped profile.

58. (previously presented) A semiconductor device according to claim 56, wherein the stripe groove has a U shaped profile.

59. (currently amended) A semiconductor device according to claim 56, further comprising an auxiliary stripe groove formed on the ~~second main surface of the structure~~ first chip surface, wherein the stripe groove and the auxiliary stripe groove intersect at an off-center point.

60. (currently amended) A semiconductor device according to claim 56, further comprising an auxiliary stripe groove formed on the ~~second main surface of the structure~~ first chip surface, wherein the auxiliary stripe groove is parallel to the stripe groove, and wherein the auxiliary stripe groove divides the ~~second main~~ first chip surface asymmetrically.

61. (previously presented) A semiconductor device according to claim 56, wherein the terminals are arranged in a plurality of rows.

62. (previously presented) A semiconductor device according to claim 61, wherein the stripe groove is formed at a position corresponding to one of the rows of the terminals.

63. (currently amended) A semiconductor device comprising:

a semiconductor chip having a first chip surface including a plurality of sides and a second chip surface on which a plurality of electrode pads are formed;

a molding resin structure covering the first chip surface of the semiconductor chip, the molding resin structure having a first main surface and a second main surface opposite to the first main ~~surface, the second main surface having four sides~~ surface;

a plurality of terminals formed on the first main surface of the structure, the terminals being electrically connected to the electrode pads, respectively; and

a steplike section formed on one of the sides of the ~~second main surface of the structure~~ first chip surface.

64. (currently amended) A semiconductor device according to claim 63, wherein a thickness ~~of the structure~~ at the steplike section becomes smaller approaching the one of the edges.

65. (currently amended) A semiconductor device according to claim 63, further comprising an auxiliary steplike section formed on another one of the sides of the ~~second main surface of the structure~~ first chip surface, wherein the auxiliary steplike section and the steplike section intersect at a corner of the ~~main~~ first chip surface.

66. (previously presented) A semiconductor device according to claim 63, wherein the terminals are arranged in a plurality of rows.

67. (currently amended) A semiconductor device comprising:

a semiconductor chip having a first chip surface, including a plurality of sides and a second chip surface on which a plurality of electrode pads are formed, the first chip surface having a first roughness;

a sealing resin structure covering the second chip surface of the semiconductor chip, the sealing resin structure having a first main surface and a second main surface ~~opposite to the first main surface, the second main surface having a first roughness~~;

a plurality of terminals formed on the first main surface of the structure, the terminals being electrically connected to the electrode pads, respectively; and

a stripe portion formed on the ~~second main surface of the structure~~ first chip surface, the strip portion having a second roughness that is coarser than the first roughness, wherein the stripe portion divides the ~~second main~~ first chip surface asymmetrically.

68. (previously presented) A semiconductor device according to claim 67, wherein the stripe portion has a groove.

69. (previously presented) A semiconductor device according to claim 68, wherein the groove has a V shaped profile.

70. (previously presented) A semiconductor device according to claim 68, wherein the groove has a U shaped profile.

71. (currently amended) A semiconductor device according to claim 67, further comprising an auxiliary stripe portion formed on the ~~second main surface of the structure~~ first chip surface, the auxiliary strip portion substantially having the second roughness, wherein the stripe portion and the auxiliary stripe portion intersect at an off-center point.

72. (currently amended) A semiconductor device according to claim 67, further comprising an auxiliary stripe portion formed on the ~~second main~~ first chip surface ~~of the structure~~ in parallel with the strip portion, the auxiliary strip portion substantially having the second roughness, wherein the auxiliary stripe portion divides the ~~second main~~ first chip surface asymmetrically.

73. (previously presented) A semiconductor device according to claim 67, wherein the terminals are arranged in a plurality of rows.

74. (previously presented) A semiconductor device according to claim 73, wherein the stripe portion is formed at a position corresponding to one of the rows of the terminals.

75. (previously presented) A semiconductor device according to claim 56, wherein the stripe groove has a function of indicia for recognizing an orientation of the semiconductor device.

76. (previously presented) A semiconductor device according to claim 63, wherein the steplike section has a function of indicia for recognizing an orientation of the semiconductor device.

77. (previously presented) A semiconductor device according to claim 67, wherein the stripe portion has a function of indicia for recognizing an orientation of the semiconductor device.

Claims 78 and 79 (cancelled).

80. (previously presented) A semiconductor device according to claim 63, wherein at least one of the sides of the ~~second main surface of the structure~~ first chip surface lacks a steplike section.